AMENDMENT TO THE CLAIMS

This listing of claims will replace all prior versions of claims in the application.

Listing of Claims:

1. (Currently Amended) An apparatus to multiplex multiple bits per bit input comprising:

a first passgate circuit coupled to receive a first plurality of input signals and a first plurality of select signals~~, wherein the first passgate circuit includes~~ corresponding to selecting one of the first plurality of input signals as output onto a first output node~~, and wherein the first passgate circuit is configured to output a first voltage on the first output node responsive to an assertion of a first select signal of the first plurality of select signals, the first voltage indicative of a corresponding one of the first plurality of input signals~~; ~~and~~

a first default circuit coupled to receive the first plurality of select signals and ~~coupled to the first output node, wherein the first circuit is~~ configured to output a ~~second~~ default voltage onto the first output node~~, responsive to each of the first plurality of select signals being deasserted~~ if none of the first plurality of input signals is to be selected as output onto the first output node;

a second passgate circuit coupled to receive a second plurality of input signals and a second plurality of select signals corresponding to selecting one of the second plurality of input signals as output onto a second output node;

a second default circuit coupled to receive the second plurality of select signals and configured to output a default voltage onto the second output node, if none of the second plurality of input signals is to be selected as output onto the second output node; and

an output logic circuit coupled to the first and second output nodes to receive a selected output from one of the first or second passgate circuits as a first input and the default voltage from a non-selected passgate circuit as a second input, the output logic circuit to generate an output onto a third output node that is to correspond to the selected input signal.

2. (Currently Amended) The apparatus as recited in claim 1, wherein the first and second default circuits each comprise a logic gate to receive corresponding select signals and to drive a transistor in response to the select signals ~~further comprising:~~

~~a second passgate circuit coupled to receive a second plurality of input signals and a second plurality of select signals, wherein the second passgate circuit includes a second output node, and wherein the second passgate circuit is configured to output a third voltage on the second output node responsive to an assertion of a second select signal of the second plurality of select signals, the third voltage indicative of a corresponding one of the second plurality of input signals;~~

~~a second circuit coupled to receive the second plurality of select signals and coupled to the second output node, wherein the second circuit is configured to output a fourth voltage on the second output node responsive to each of the second plurality of select signals being deasserted; and~~

~~a third circuit coupled to receive the voltages on the first output node and the second output node as inputs, wherein the third circuit is configured to output an output signal responsive to its inputs~~.

3. (Currently Amended) The apparatus as recited in claim 2, wherein a plurality of first passgate circuits corresponding to first same bit positions are coupled to the first default circuit and a plurality of second passgate circuits corresponding to second same bit positions are coupled to the second default circuit and in which each default circuit to control output of default voltage onto respective individual first and second output nodes for the plurality of passgate circuits ~~wherein the second voltage represents a logical one, and wherein the third circuit performs an AND function on the voltages on the first output node and the second output node~~.

4. (Currently Amended) The apparatus as recited in claim 3 wherein the ~~third~~ output logic circuit comprises ~~a~~ NAND ~~gate~~ logic.

5. (Currently Amended) The apparatus as recited in claim 2 wherein the ~~second voltage represents a logical zero, and wherein the third~~ first and second default circuits each performs an OR function on the ~~voltages on the first output node and the second output node~~ respective plurality of select signals.

6. (Currently Amended) The apparatus as recited in claim 5 wherein the ~~third~~ output logic circuit comprises ~~a~~ NOR ~~gate~~ logic.

7. (Currently Amended) The apparatus as recited in claim 2 further comprising:

a third passgate circuit coupled to receive a third plurality of input signals and a third plurality of select signals~~, wherein the third passgate circuit includes~~ corresponding to selecting one of the third plurality of input signals as output onto a third output node~~, and wherein the third passgate circuit is configured to output a fifth voltage on the third output node responsive to an assertion of a third select signal of the third plurality of select signals, the fifth voltage indicative of a corresponding one of the third plurality of input signals~~; and

a ~~fourth~~ third default circuit coupled to receive the third plurality of select signals and ~~coupled to the third output node, wherein the fourth circuit is~~ configured to output a ~~sixth~~ default voltage onto the third output node~~, responsive to each of the third plurality of select signals being deasserted~~ if none of the third plurality of input signals is to be selected as output onto the first output node, the third default circuit comprises a logic gate to receive the third plurality of select signals and to drive a transistor in response to the third plurality of select signals;

8. (Currently Amended) The apparatus as recited in claim ~~1~~ 7 wherein ~~the first circuit comprises a transistor and a logic gate~~ a plurality of third passgate circuits corresponding to third same bit positions are coupled to the third default circuit and in which the third default circuit to control output of default voltage onto the third output nodes for the plurality of third passgate circuits.

9. (Currently Amended) The apparatus as recited in claim ~~8~~ 2 wherein the driven transistors ~~is~~ are an N-type Metal-Oxide-Semiconductor transistor.

10. (Canceled)

11. (Currently Amended) The apparatus as recited in claim ~~8~~ 2 wherein the drive transistors ~~is~~ are an P-type Metal-Oxide-Semiconductor transistor.

12-19. (Canceled)